High-sensitivity chip calorimeter platform for sub-nano watt thermal measurement

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Abstract

High sensitivity, on-chip calorimeter platform using V_2O_5 thin film thermistor was developed. Integration of a V_2O_5 thermistor with a high temperature sensitivity of ~2.2%/K with a vacuum insulated, suspended SiN membrane structure enabled a low thermal conductance of 12 μW/K and a direct detection of 10 nW of heat with an estimated detection limit of 570 pW. We also investigated the feasibility of integrating the platform with a microfluidic system, and suggest that, based on numerical simulations, a further 5-fold lowering of detection limit may be possible.

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1. Introduction

Calorimetric measurement of the heat has several unique advantages over other methods of measurements for biological processes; it measures metabolic energy directly without labeling, and does not require sample preparation steps such as immobilization [1–3]. However, the sensitivity of calorimeters reported so far has been relatively low such that measuring the cellular metabolic rate required an ensemble average of ~10^3–10^6 cells, as reliable measurement of basal metabolism of a single mammalian cell requires a resolution of a few picowatts [4]. Furthermore, continuous measurement with living cells, not to mention a single cell, is quite difficult with present calorimeter technologies. Thus, there have been many attempts to develop an on-chip platform for such a calorimeter [5–7]. Chip calorimeters can provide high sensitivity and fast response due tiny thermal mass and conductance. They can be mass produced by leveraging the semiconductor processing infrastructure. Furthermore, such a platform can be integrated with a microfluidic system [8,9], providing the ability to control the environment of the reaction volume for a stable and reproducible operation.

The power resolution of chip calorimeter can be represented by product of their thermal conductance and temperature resolution (∆P = G ∆T). Therefore the engineering of the chip calorimeter devices have been focused to achieve high sensitivity thermometry and low thermal conductance. Chip calorimeters achieve low thermal conductance by reducing the size of thermal conduction path: They typically have μm to mm scale calorimeter chambers and thin membrane structure such as suspended SiN that provides thermal insulation. Even though the membrane structure provides relatively decent thermal insulation, the substrate and microfluidic components represent too large of heat conduction paths to achieve high resolution. In this paper, we report on developing a chip calorimeter platform based on V_2O_5 thin film thermistors for high sensitivity thermometry and thermal engineering to achieve better resolution. A thin film thermistor was chosen as it can easily detect small changes of temperature with exponential changes of resistance. Furthermore, it can be fabricated on a microscale sensing area without sacrificing thermal insulation [10]. V_2O_5 was chosen as the thermistor material due to its large temperature coefficient of resistance (TCR, defined to be (1/ρ) (dρ/dT) = (d(ln ρ))/dT) and relatively low electric noise property. In addition, V_2O_5 has a homogeneous TCR without metal-insulator-transition (MIT) within the temperature range of interest (~100 °C) [11]. Finally, a suspended SiN membrane structure was chosen to reduce both the thermal conductance and the heat capacitance contribution from the under-
lying Si substrate, and to enable eventual vacuum insulation. We found that by controlling the oxygen content during RF sputter deposition, V$_2$O$_5$ thin film with a TCR of $-2.2\%$/K could be formed after an anneal at 300°C. This high TCR, when combined with a vacuum insulated, suspended SiN membrane structure with a low thermal conductance of 12 μW/K, enabled a direct detection of 10 nW of heat with an estimated detection limit of 570 pW. Finally, we demonstrated the feasibility of integrating the platform with a microfluidic system, and, suggested that, based on numerical simulations, a further 5-fold lowering of detection limit may be possible, which would enable direct calorimetric measurements of sub-nanowatt cellular metabolic rate.

2. Experimental

2.1. Vanadium pentoxide thin film thermistor fabrication

A 200 nm thick V$_2$O$_5$ film was deposited at room temperature on a Si wafer with 200 nm SiN layer via RF sputtering using V$_2$O$_5$ target (99.9% purity) with Ar and O$_2$ gas flow. The compositions of the deposited films were analyzed using Rutherford Backscattering Spectroscopy (data not shown). Post-deposition annealing at 300°C for 30 min in flowing O$_2$ was performed to crystallize the as-deposited amorphous film. Fig. 1(a) shows the X-ray diffraction (XRD) spectra of the films after annealing. We found that for crystallization, controlling the stoichiometry of the vanadium oxide is critical. The strongest XRD peaks corresponding to the Shcherbinaite V$_2$O$_5$ phase were observed from the stoichiometric V$_2$O$_5$ film, while the vanadium-deficient film remained amorphous even after annealing. The formation of crystalline V$_2$O$_5$ film was further confirmed by its X-ray photoelectron spectrum. As shown in Fig. 1(b), the oxidation states of vanadium atoms were consistent with V$_2$O$_5$ phase.

2.2. On-chip calorimeter fabrication

In order to achieve the low thermal conductance required for high sensitivity calorimeters, it is important to carefully engineer the thermal insulation, including the design of the device and selection of the materials. For this purpose, we employed a SiN membrane structure formed by back-etching the entire wafer through a window in the backside SiN layer. First, windows were opened in the back side SiN layer by standard photolithography and dry etching. Afterward, the heater and electrode layer was formed by depositing a 50 nm thick gold thin film, with a 5 nm thick chromium layer acting as the glue layer, on the SiN layer. After the lift-off process to form the heaters and electrode, a 200 nm thick V$_2$O$_5$ thin film thermistor was created on top of the gold electrodes using deposition and lift-off. The thermistor was surrounded by the gold heater to enable power calibration. Finally, wet chemical etching of back side bulk silicon substrate using 30% KOH solution was performed to selectively remove the Si substrate under the sensing element, thus forming a suspended membrane structure. A schematic description of the fabricated thermistor platform is shown in Fig. 2(a).

Fig. 2(b) and (c) shows the optical microscope image of the fabricated platform and its circuit diagram, respectively. The thermistors were wired in a Wheatstone bridge configuration on the chip to provide accurate measurement [12]. Each thermistor is built on individual membrane structure to balance thermal transport, which allows rejection of base line temperature fluctuation. Two heaters are built next to the thermistors for calibration of thermal conductance. Their configuration is also identical in sensing area and reference area. For calibration electric power was applied to only one side of the heater, but the extra heater on the reference will help matching the thermal conductance.

3. Results and discussion

3.1. Temperature sensitivity of V$_2$O$_5$ thermal sensor

The temperature dependence of electrical resistance of fabricated V$_2$O$_5$ thin film thermistor was investigated using a temperature-controlled probe station (HP4156C, Agilent Technologies). As shown in Fig. 3, we measured the temperature dependence of the resistance of V$_2$O$_5$ thin film thermistor between 0 and 90°C. The heating and cooling cycle display no MIT and small hysteresis of 2.08°C. The hysteresis increases with temperature ramping speed, which we attribute to insufficient temperature stabilization on the probe station. The TCR was $-2.2\%$/K, which is typically reported V$_2$O$_5$ TCR for image-quality bolometers [13].

3.2. Sensitivity enhancement using vacuum insulation

For a high sensitivity, however, heat loss must be minimized as well. For the fabricated thermistor, the heat conduction through the air is the most significant factor due to its high surface to volume ratio. To investigate the effect of heat conduction through the air, the sensing area was heated with a fixed power of 1 μW while placed inside a vacuum chamber. By measuring the steady state temperature difference between the sensing thermistor and the reference thermistor, the heat conduction can be readily extracted using the heat balance equation $P = G \times \Delta T$ where P, G, and $\Delta T$ are the power, thermal conductance, and the temperature difference in steady state, respectively. The results are shown in Fig. 4. We found that the heat conduction through air contributes as much as 90% of the total heat loss, indicating that vacuum insulation was
Fig. 2. (a) Schematic representation of fabrication process of a sensor platform in cross-sectional view. (b) Photograph of a fabricated chip calorimeter. For the measurement of thermistor resistance change, four identical sensors are interconnected to form an on-chip Wheatstone bridge circuit. Gold heater was fabricated to calibrate power resolution of a thermistor (Zoom-up image). (c) Single element varying Wheatstone bridge circuit diagram and thermal conductance calibration measurement system.

Fig. 3. Temperature dependence of electrical resistivity of V$_2$O$_5$ thin film thermistor.

3.3. Thermal conductance and power resolution

We first measured the dynamic response of the device by applying 1 $\mu$W square wave to the heater. As shown in Fig. 5(a), a corresponding temperature change of 81 mK that was synchro-
Fig. 4. Device thermal conductance change as a function of air pressure. Vacuum insulation provides 10-fold resolution enhancement.

![Graph showing device thermal conductance change](image)

Fig. 5. (a) Dynamic response of device by applying 1 μW square wave to the heater. Thermal conductance and thermal time constant were measured to be 12 μW/K and 22 ms, respectively. (b) Direct measurement of thermal power allows reliable measurement down to 10 nW of heater power. Inset shows the calorimeter response to 10 nW square wave heating (frequency 4 Hz).

Fig. 5. (b) inset. Ultimately, under the assumption of the absence of any noise from the electronic system, the power resolution of the device is limited by its intrinsic Johnson noise, given by

\[ V_{\text{noise}} = \sqrt{4kTf} \]

For the 80 kΩ thermistor used in this study, the Johnson noise is calculated to be 36 nV/√Hz. Based on noise equivalent temperature difference of 16 μW (NETD = \[ V_{\text{noise}} / T \]), where TCR = 2.2%, \[ V_{\text{m}} = 0.2 \text{ V} \], and the Vnoise = 36 nW), the temperature resolution of the device is estimated to be 48 μK (with signal-to-noise ratio 3:1) in an estimated bandwidth of 1 Hz. Thus, the ultimate power resolution, which is corresponded to three times the noise equivalent power (NEP), is estimated to be 570 pW.

We note here that we cannot yet achieve such a high resolution due to the excess noise, as can be seen in Fig. 5(a) and in the inset of Fig. 5(b). Spectral analysis of the noise spectrum indicated that the major portion of the noise is the low-frequency noise and the 60 Hz power line noise and its harmonics (data not shown). As the intrinsic 1/f noise from Vanadium oxide was reported to be very small [11], we expect that much higher resolution can be reached with better isolation and noise-reduction techniques such as lock-in amplifiers.

4. Numerical investigation of microfluidic integration

Above results, however apply to the bare thermistor element only. In a real chip calorimeter, such a thermistor element needs to be integrated with a microfluidic system that includes channels, liquids, and other layers, all of which can significantly increase the overall thermal conductance and degrade the power resolution. Thus, in order to investigate the practically achievable power resolution, we numerically simulated the heat conduction property of the platform integrated with two types of microfluidic system: one with conventional, “tunnel-type” channels formed in a thick, continuous layer of Polydimethylsiloxane (PDMS), and another with “tube-type” channels formed by a thin layer of parylene. Parylene is a conformal protective polymer coating material with excellent thermal, mechanical, and chemical stability that enables fabrication of thin-film, microfluidics with low heat capacitance and thermal conductance [14]. Fig. 6(a) and (b) shows schematic descriptions of the “tunnel-type” and “tube-type” microfluidics systems, respectively. The structure includes SiN membrane, heater, thermistor, fluidic channel, and water inside the channel. The PDMS layer is assumed to be 1 mm thick, and the parylene layers are assumed to be 3 μm thick. Both systems have a fluidic chamber at the center of the membrane having a volume of 3.0 nL (600 μm (width) × 500 μm (length) × 10 μm (height)), and connected to channels with a width of 50 μm and height of 10 μm. We also assume that the entire fluidic system is filled with water. Heating power of 1 μW is applied to the fluidic chamber and the end the membrane is set to be constant temperature. We assumed the application of vacuum and the heat transport is only by conduction through the device materials. Fig. 6(c), (d), and (e) shows the temperature distribution of bare platform, PDMS microfluidic system, and parylene microfluidic system, respectively. As expected, application of a thick PDMS layer results in more than an order of magnitude increase in heat conduction such that any advantage of the platform is lost. With a parylene microfluidic system, however, the thermal conductance of the entire platform remains very low, increasing by only 23% over the value of the bare platform indicating that the narrow, long channel effectively insulates the chamber such that the thermal conduction is still dominated by the electrode and the SiN membrane. This is further confirmed by the fact that a drastic, 5-fold improvement of power resolution can be obtained by etching the sides of the membrane and microfluidic channels to form a bridge structure suspended only from the two ends of the
SiN membrane, as shown in Fig. 6(f). Such 5-fold increase of thermal insulation should enable a theoretical resolution of \(\sim 150 \text{ pW} \).

5. Conclusion

In conclusion, we have demonstrated the fabrication of highly sensitive, vanadium oxide thin film thermistor platform for use in on-chip calorimeters. From XRD and XPS data we confirmed the vanadium oxide has mainly V_2O_5 phase. The V_2O_5 thermistor has high temperature sensitivity of \(-2.2\%/K\). Such a high sensitivity, combined with a vacuum insulated, suspended SiN membrane structure that can provide a low thermal conductance of 12 \(\mu\text{W/K} \), provides a resolution of 570 pW. Numerical simulations indicate that such a high resolution can be maintained. We investigated the feasibility of integrating the platform with a microfluidic system using numerical simulations, and suggest that, based on numerical simulations, a further 5-fold lowering of detection limit may be possible by constructing a suspended bridge structure.

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References

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