Effect of hydrogenation on the memory properties of Si nanocrystals obtained by inductively coupled plasma chemical vapor deposition

Young-Kwan Cha, Sangjin Park, a,b) Youngsoo Park, and In-Kyeong Yoo
Nano Devices Lab, Samsung Advanced Institute of Technology, P. O. Box 111, Suwon, Kyonggi 440-600, Korea

Daigil Cha and Jung H. Shin
Department of Physics, Korea Advanced Institute of Science and Technology, 373-1 Kusung-dong, Yusung-gu, Daejon 305-701, Korea

Suk-Ho Choic)
Department of Physics and Applied Physics, College of Electronics and Information, Kyung Hee University, Yongin 449-701, Korea

(Received 14 September 2005; accepted 3 October 2006; published online 15 November 2006)

Effect of hydrogenation on memory properties has been studied for metal-oxide-semiconductor (MOS) structures with Si nanocrystals fabricated using inductively coupled plasma chemical vapor deposition and subsequent annealing. Hydrogenation induces a drastic increase of a dip in the quasistatic capacitance-voltage (C-V) curve of the MOS capacitor, caused by the reduction of the interface states due to hydrogen passivation. This is consistent with high-frequency C-V measurements showing more well-defined curves with less distortion in hydrogenated samples. After hydrogenation, the MOS device shows a significantly larger decrease of flatband voltage shift in electron charging than in hole charging, indicating more effective passivation of the defect states related to the electron charging. A longer retention time is found for electron charging after hydrogenation, but almost no change of charge loss rate for hole charging. These results suggest that an asymmetry exists in the effect of hydrogenation between electron and hole storage.

Si-nanocrystal (Si-NC) memory devices have recently attracted much attention for high-density low-power memory application,1,2 because they have many advantages such as smaller leakage current and inherent scalability even down to single electron devices in comparison to current poly-Si floating gate memories.3 Among the various fabrication methods for Si NCs embedded in a SiO2 film, chemical vapor deposition (CVD) of silicon-rich SiOx followed by annealing has been utilized to form Si NCs without compromising the integrity of the gate oxide and the quality of the interface with the substrate. This process has several advantages such as good passivation of the Si-Nc surface, easier site control, and uniform size distribution, but the CVD films include a lot of defect sites related to suboxides and dangling bonds.

It has been suggested that charge storage in Si-NC based metal-oxide-semiconductor (MOS) structures is influenced by several mechanisms including quantum confinement effect and interface/defect states.4 On the other hand, Si NCs can be passivated by hydrogen, which has a significant effect on the photoluminescence intensity by increasing it by up to an order of magnitude.5–7 This has been attributed to hydrogen passivation of nonradiative defect centers such as Si dangling bonds located at the NC surface.6–8 The interface/defect states in MOS structures are also expected to be considerably reduced by hydrogenation passivation, improving the memory effect. But almost no detailed study has been done on this topic. It is also important to distinguish charge storage in Si NCs from that in interface/defect states for understanding the memory effects in MOS structures containing Si NCs.

In this letter, we employ inductively coupled plasma CVD (ICP-CVD) and thermal annealing to fabricate MOS structures containing Si NCs and study the effect of hydrogen passivation on their nonvolatile memories by using quasistatic and high-frequency capacitance-voltage (C-V) measurements, high-resolution transmission electron microscopy (HRTEM), and x-ray photoemission spectroscopy (XPS).

For a MOS structure containing Si NCs, a tunneling SiO2 layer of 2 nm was first thermally grown on p-type (100) Si wafers in a conventional furnace. Subsequently, a 4 nm SiOx was grown on top of the oxide layer in an ICP-CVD reactor at room temperature. In this process, a mixed gas of SiH4 and O2 with a pressure of 14 mTorr was introduced into the reactor. The relative oxygen content was controlled by varying the oxygen gas pressure. The stoichiometry of the SiOx films was analyzed by XPS, and their x values are summarized in Table I. Finally, a control oxide of 7 nm was deposited to form a (SiO2/SiOx/SiO2) sandwich structure. After deposition, the samples were annealed at 900 °C for 30 min in an ultrapure Ar ambient to form Si NCs in the SiOx layers. The HRTEM images of these

| TABLE I. Value of x determined by XPS for each flow rate ratio of O2/SiH4. |
|----------------------|--------|-------|-------|-------|
| O2/SiH4 flow rate ratio | 0.3    | 0.7   | 0.9   | 1.1   |
| Stoichiometry x        | 0.7    | 1.2   | 1.5   | 2.0   |
samples confirmed the presence of Si crystallites of approximately 2–3 nm, as shown in Fig. 1.

2% Nd-doped Al electrodes with a diameter of 100 μm were deposited on the samples in vacuum for C-V measurements of MOS capacitors. Some of the samples were hydrogenated for the passivation of the Si dangling bonds at 250 °C for 30 min in forming gas (50% H2 in Ar). Hydrogenation was performed at a relatively low temperature because it was done after the deposition of electrodes on the samples. Quasistatic C-V (QSCV) curves were measured by using an Agilent 4156C, and high-frequency C-V measurements were carried out by using an Agilent 4288A C-V meter with a frequency of 1 MHz and a modulation signal amplitude of 100 mV.

Figure 2 compares QSCV characteristics of the MOS capacitors with $x=1.2$ after various sample treatments. The small dip in the QSCV curve of the as-deposited sample is characteristic of a Si/SiO2 interface with a very high interface trap density. The QSCV of the capacitor exposed to the annealing exhibits an increase of the dip reflecting a decreasing amount of interface states. An interesting feature in this characteristic is the emergence of a peak in the C-V response in the vicinity of the strong inversion, which is an indication of an interface state distribution that peaks at a specific energy. By subsequent hydrogenation the minimum of the QSCV curve moves even more downward, which is believed to be caused by the reduction of the interface states due to hydrogen passivation. The peak near the inversion region still exists, but its height is severely reduced. However, this peak is not observed when the hydrogenation is done without previous annealing. This indicates that the peak is solely due to the annealing. It has been previously reported that the oxidation process can produce an interface state distribution at the Si–SiO2 interface. We suggest that while the phase separation of the SiOx layer progresses during the annealing process, interface states between Si NCs and the SiO2 matrix are formed, responsible for the peak in the QSCV.

Figure 3 shows the effect of hydrogenation on the high-frequency C-V (HFCV) hysteresis for the MOS capacitors with annealed SiOx layers of different stoichiometries $x$. Table I summarizes the correlation of the O2/SiH4 flow rate ratio with the $x$ value. The accuracy of the $x$ value determined by XPS is about 5%. After hydrogenation, the C-V curves are more well defined with much less distortion irrespective of the $x$ value, indicating the reduction of the interface states by hydrogenation passivation, consistent with the QSCV results in Fig. 2. A decrease of the width in the C-V hysteresis after hydrogenation is also clearly observed in Fig. 3. Several models have been proposed to explain charge storage in MOS structures containing Si NCs, the two most dominant being charge storage in the Si NCs and charge storage in defect states. The latter is generally attributed to structural defects at the Si NCs/SiO2 and SiO2/Si substrate interfaces. The defect states in such samples are expected to be considerably reduced by hydrogenation passivation, reducing $\Delta V_{FB}$. In Fig. 3, the SiOx with $x=2.0$ is almost stoichiometric SiO2. So, the device is a MOS structure with a SiO2 containing no nanocrystals, which has almost no flatband voltage shift before and after hydrogenation. This result suggests that the memory effect from the interface states at SiO2/Si is very small compared to that from Si NCs or that from the interface states at Si NCs/SiO2.

In Fig. 3, the flatband voltage shift $\Delta V_{FB}$ due to electron or hole charging can be separately estimated from the shift of the C-V curve in the positive or negative direction with respect to the curve with almost no hysteresis. In this case the curve with $x=2.0$. These results are summarized in Fig. 4. There is a small decrease in $\Delta V_{FB}$ with increasing $x$ value up to 1.2, but above this, the voltage shift is sharply reduced irrespective of the type of charging.

It should be noted that an asymmetry of reduction in the memory window exists between the electron and hole stor-
age after hydrogenation. In Fig. 4, after hydrogenation, the MOS device shows a significantly large decrease of $\sim 4.2$ V in $\Delta V_{FB}$ due to the electron charging at an $x$ value of 0.7, but in the hole charging, it shows a much smaller decrease of $\sim 1.2$ V. This indicates that the hydrogenation passivates more efficiently the defect states for electron charging than those for hole charging. This is contrasted with the observation that the hole trap states at the interface of amorphous Si quantum dots ($a$-Si QDs)/substrate is more efficiently reduced by hydrogen passivation.\textsuperscript{12} After hydrogenation, both types of charging show a similar trend of variation in $\Delta V_{FB}$ depending on the $x$ value, as shown in Fig. 4. From these results, it is reasonable to assume that Si NCs play a major role in charging behaviors after hydrogenation.

Figure 5 shows the effect of hydrogenation on the retention characteristics for the same samples used in Figs. 3 and 4. These data were obtained by studying the transient of the voltage shift $\Delta V_{FB}$ after programming pulses of ($\pm 10$ V, 1 s). After hydrogenation, the charge loss rate is reduced for electron charging, but almost no change of charge loss rate is found for hole charging. It is widely accepted that the charge loss rate of defect states is higher than that of Si NCs.\textsuperscript{3,13} As explained in Fig. 4, after hydrogenation, the retention behaviors of stored electron charge are dominated by Si NCs, resulting in a smaller loss rate for electron charging, as shown in Fig. 5. There has been a similar report that a better improvement of retention for electron charging than for hole charging is observed in hydrogen-passivated $a$-Si QDs embedded in silicon nitride.\textsuperscript{12}

In conclusion, MOS structures containing Si NCs were fabricated by ICP-CVD and subsequent annealing to investigate the effect of hydrogenation on their memory properties. The hydrogenation passivation of the interface states was confirmed by a drastic increase of a dip in the QSCV curve as well as by less distortion in the HFCV curve. It was found that an asymmetry exists in the effect of hydrogenation between the electron and hole storage. After hydrogenation, the MOS capacitor exhibited a larger decrease in $\Delta V_{FB}$ and less charge loss rate for electron charging than for hole charging, meaning more efficient passivation of electron-storage related defect states.

This work was performed using FE-TEM (JEM-2100F, Jeol, Japan) installed at Korea Basic Science Institute.